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Study truth table of Half Subtractor using Aim-Spice

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***Abstract*—The truth table of half subtractor is studied by using aims-spice software. The output of half subtracor is subtraction and borrow. The circuit for both subtraction and borrow is separately designed .**

I. Introduction

THE Subtractor circuits take two binary numbers as input and subtract one binary number input from the other binary number input. Similar to adders, it gives out two outputs, difference and borrow (carry-in the case of Adder). There are two types of subtractors.

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow). An important point worth mentioning is that the half substractor diagram aside implements (b-a) and not (a-b) as borrow is calculated from equation

II. Main Part

Truth Table:-

Inputs		Outputs	
A	**B**	**D_i(Difference)**	**B_o(Borrow)**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig. 1. Truth Table of half subtractor

III. Equation

By Using K-map for subtraction and borrow :-

DIFFRENCE = A'.B + A.B'

BORROW = A'.B

The fig. of half subtractor's subtraction and borrow is show in fig2

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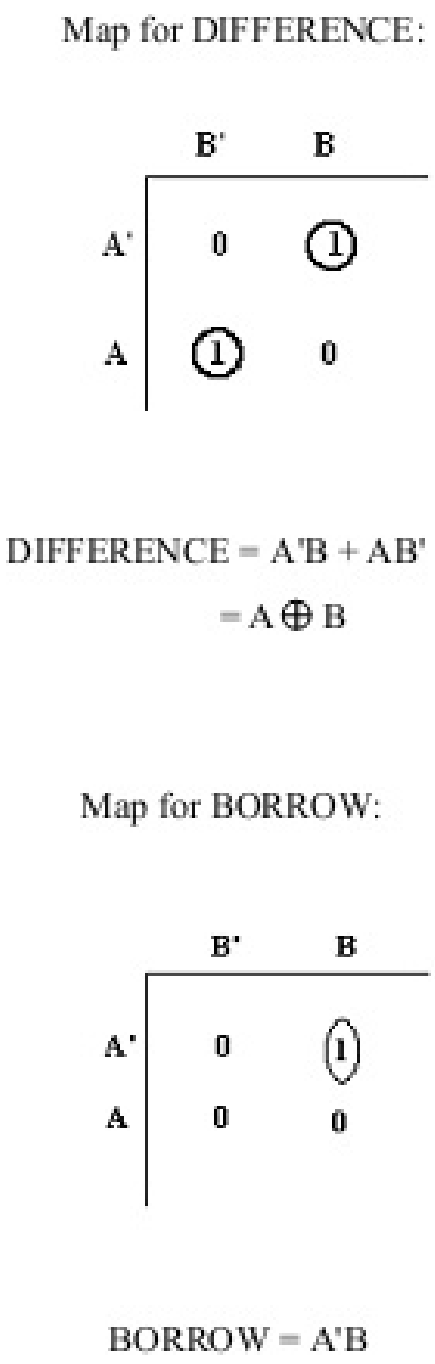

Fig. 2. K-map for subtraction and borrow.

IV. Logic Diagram

Logic diagram of half subtractor
The fig. of half subtractor is shown in fig3

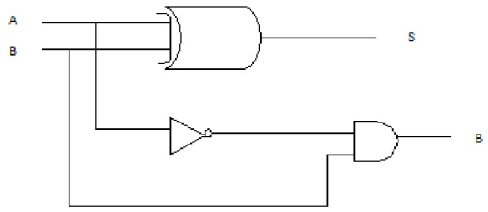

Fig. 3. Logic diagram of half subtractor

V. Cmos Circuit

CMOS diagram of exor output

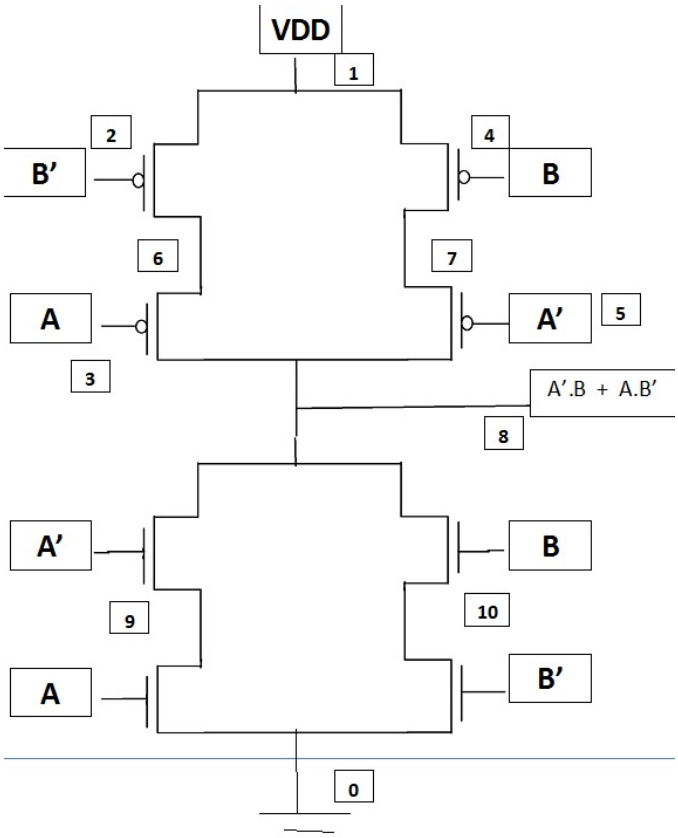

Fig. 4. Cmos diagram of half subtractor exor

CODE for exor:-
cmos exor
vdd 1 0 dc 2
va 2 0 dc 0.0 pulse(0 2 0 0 0 20ns 60ns)
vb 3 0 dc 0.0 pulse(0 2 0 0 0 30ns 60ns)
vc 4 0 dc 0.0 pulse(0 2 0 0 0 20ns 60ns)
vd 5 0 dc 0.0 pulse(0 2 0 0 0 20ns 60ns)
m1 6 2 1 1 mp l=4u w=8u
m2 8 3 6 1 mp1 l=4u w=8u
m3 7 4 1 1 mp2 l=4u w=4u
m4 8 5 7 1 mp3 l=4u w=8u
m5 8 5 9 0 mn l=4u w=4u
m6 9 3 0 0 mn1 l=4u w=4u
m7 8 4 10 0 mn2 l=4u w=4u
m8 10 2 0 0 0 mn3 l=4u w=4u
.model mp pmos
.model mp1 pmos
.model mp2 pmos
.model mp3 pmos
.model mn nmos
.model mn1 nmos
.model mn2 nmos
.model mn3 nmos

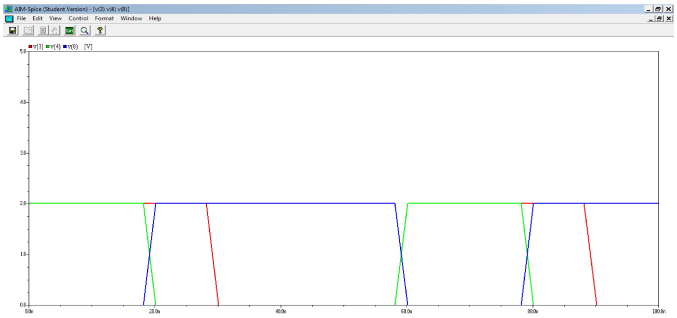

Fig. 5. Transfer characteristics of exor

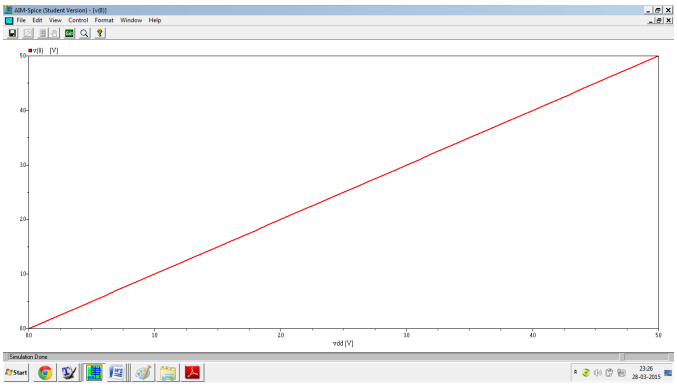

Fig. 6. DC characteristics of exor

CMOS diagram of borrow output
CODE for borrow:-
cmos borrow
vdd 1 0 dc 2
va 2 0 dc 0.0 pulse(0 2 0 0 0 20ns 40ns)
vb 3 0 dc 0.0 pulse(0 2 0 0 0 20ns 40ns)
m1 4 2 1 1 mp l=4u w=8u
m2 5 3 4 1 mp1 l=4u w=8u
m3 5 2 0 0 mn l=4u w=4u
m4 5 3 0 0 mn1 l=4u w=4u
.model mp pmos

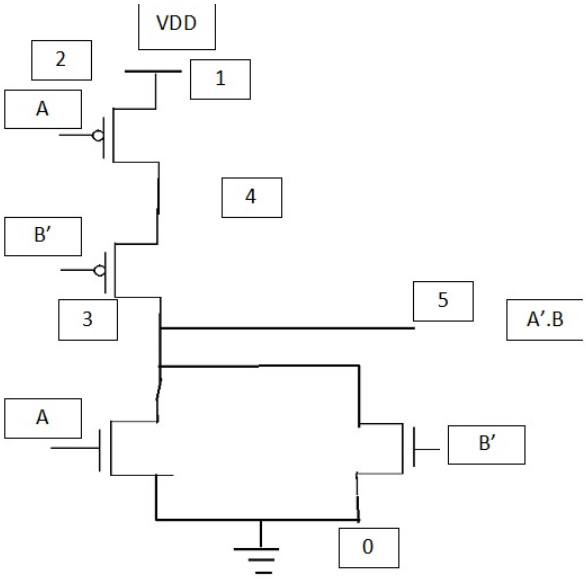

Fig. 7. Cmos diagram of half subtractor borrow

.model mp1 pmos
.model mn nmos
.model mn1 nmos

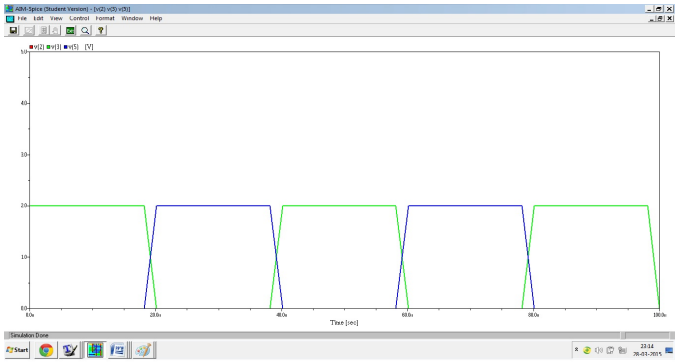

Fig. 8. Transfer characteristics of borrow

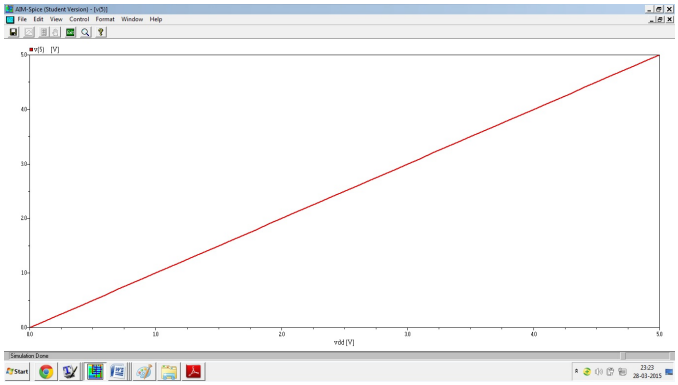

Fig. 9. DC characteristics of borrow

VI. Conclusion

We concluded that truth table of half subtractor is implemented by Aim-Spice.The no change in rise time,fall time and propagation time delay to scaling.

References

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